That which is claimed is:

1. A semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a gate finger, wherein a pitch between the gate fingers is varied in a predetermined pattern between the gate fingers so as to provide a non-uniform pitch between the gate fingers.

2. The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a substantially uniform junction temperature to a substantial majority of the gate fingers when in operation.

3. The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a lower peak junction temperature than a corresponding uniform gate pitch device for a particular set of operating conditions.

4. The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a substantially uniform junction temperature to all but the outermost gate fingers of the device when in operation.

5. The semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arranged in a linear array.

6. The semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arrange in a two dimensional array and wherein the non-uniform pitch gate fingers are provided in at least one of the two dimensions of the two dimensional array.

7. The semiconductor device of Claim 6, wherein the non-uniform pitch gate fingers are provided in both dimensions of the two dimensions of the two dimensional array.

8. The semiconductor device of Claim 1, wherein the pitch between that gate fingers is inversely related to a distance of the gate finger from a center of the device.

9. The semiconductor device of Claim 1, wherein the pitch between that gate fingers at a periphery of the device is less than a pitch between gate fingers at a center of the device.

10. The semiconductor device of Claim 1, wherein the unit cells comprise MESFET unit cells.

11. The semiconductor device of Claim 1, wherein the unit cells comprise silicon carbide semiconductor device unit cells or gallium nitride semiconductor device unit cells.

12. The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a more uniform junction temperature than a corresponding uniform gate pitch device for a particular set of operating conditions.

13. The semiconductor device of Claim 2, wherein the junction temperature does not differ by more than about 5 °C over at least 80% of the plurality of unit cells.

14. The semiconductor device of Claim 2, wherein the junction temperature does not differ by more than about 5 °C over at least 95% of the plurality of unit cells.

15. A field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region; and

a plurality of gates of the unit cells, the plurality of gates being electrically connected in parallel and having a non-uniform spacing between the gates, wherein the non-uniform spacing between the gates is provided in a pattern that provides a

lower peak junction temperature than a corresponding uniform gate pitch device for a particular set of operating conditions.

16. The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a linear array of unit cells.

17. The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a two dimensional array of unit cells.

18. The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in a single dimension of the two dimensional array.

19. The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in both dimensions of the two dimensional array.

20. The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a plurality of silicon carbide unit cells.

21. A method of controlling a peak junction temperature in a semiconductor device having a plurality of gates electrically connected in parallel, the method comprising varying a spacing between the gates.

22. The method of Claim 21, wherein the step of varying a spacing between the gates comprises varying the spacing between the gates such that gates in a central region of the device are spaced farther apart from adjacent gates than are gates in a peripheral region of the device.

23. The method of Claim 21, wherein the step of varying a spacing between the gates comprises varying the spacing between the gates linearly with distance from a central region of the device.

24. The method of Claim 21, wherein the step of varying a spacing between the gates comprises varying the spacing between the gates non-linearly with distance from a central region of the device.

25. A semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a gate finger; and

means for providing a substantially uniform junction temperature to a substantial majority of the gate fingers when in operation.

26. The semiconductor device of Claim 25, wherein the means for providing provides a junction temperature does not differ by more than about 5 °C over at least 80% of the plurality of unit cells.

27. The semiconductor device of Claim 25, wherein the means for providing provides a junction temperature does not differ by more than about 5 °C over at least 95% of the plurality of unit cells.